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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/646,922	08/25/2003	Masami Makino	031057	1951

23850 7590 10/29/2008

KRATZ, QUINTOS & HANSON, LLP
1420 K Street, N.W.
Suite 400
WASHINGTON, DC 20005

EXAMINER	
SAMS, MATTHEW C	
ART UNIT	PAPER NUMBER
2617	

MAIL DATE	DELIVERY MODE
10/29/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/646,922	MAKINO ET AL.	
	Examiner	Art Unit	
	MATTHEW SAMS	2617	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 July 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 7/9/2008 has been entered.

2. Claims 1 and 3-7 have been canceled and claim 2 has been amended.

Response to Arguments

3. Applicant's arguments filed 7/9/2008 have been fully considered but they are not persuasive.

4. In response to the applicant's argument regarding "JP 59-78654 fails to disclose a structure in which a plurality of electronic chips on the two chip mount areas is in a meshing relation within an opening formed in a frame", the examiner respectfully disagrees.

The examiner maintains the rejection because of the following reasoning:

Within the housing of a foldable electronic device, there is a limited amount of space and a finite number of operational parts to be functionally placed and it is well within the scope of one of ordinary skill in the art to find the combination of mounting locations (possibly through trial and error) that allows for the dissipation of heat (LCD

driver circuit chips [*i.e.* amplifiers] should not be mounted directly above/below each other because it can stifle heat dissipation) in order to make the device as thin as possible to be aesthetically pleasing and convenient for the user to carry, which can lead one of ordinary skill in the art to position the chips in a staggered meshing relation within the opening of the frame.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kweon et al. (US-6,925,313 hereafter, Kweon) in view of the cited prior art document JP 59-78654, hereafter document 59-78654.

Regarding claim 2, Kweon teaches a foldable electronic device (Fig. 1 [10] & Fig. 2 [20]) comprising a main body (Fig. 1 [10A]), a closure (Fig. 1 [10B]), a main display (Fig. 1 [12]), a subdisplay (Fig. 2 [22B]), a frame (Fig. 3 [24]), a chip mount area extending from the main display (Fig. 3 [27]) and a chip mount area extending from the subdisplay (Fig. 3 [28]). Kweon teaches the main body (Fig. 1 [10A]) and the closure (Fig. 1 [10B]) being connected to each other openably (Fig. 1 & 2), with the main display (Fig. 1 [12]) having a screen exposed from an inner surface of the closure (Fig. 1) and the subdisplay (Fig. 2 [22B]) having a screen exposed from the back surface of the

closure (Fig. 2), the frame (Fig. 3 [24]) being provided inside the closure (Fig. 5 [21, 22 & 24] and Col. 2 lines 48-50) and securing the main display and the subdisplay as arranged back to back (Fig. 1, Fig. 2, Fig. 3 and Col. 2 lines 40-42) with the chip mount areas being opposed to each other in an opening formed in the frame (Fig. 3) with the opposed surfaces of the respective chip mount areas having at least one portion with groups of electronic chips mounted thereon and at least one portion free of a group of electronic circuit chips. (Fig. 3 [27 & 28] & Fig. 5) Kweon teaches the chip mounting surfaces has a folded-over portion opposed to the frame and providing the chip mounting area. (Fig. 3 [27 & 28]) Kweon teaches a foldable electronic device with a frame that has an opening in a second area (Kweon Fig. 3 [24]) adjacent to a first area covered with the subdisplay and the flexible lead extending from the subdisplay is folded over on the second area (Kweon Fig. 3),

wherein the flexible lead (Kweon Fig. 3 [25 & 27]) extending from the main display (Kweon Fig. 3 [27]) is folded over toward the frame side and folded-over lead portion has a surface opposed to the frame and providing the chip mount area (Kweon Fig. 3), and

wherein the electronic circuit chips in the chip mount area of the flexible lead (Kweon Fig. 3 [25 & 28]) extending from the subdisplay (Kweon Fig. 3 [28]) and the electronic circuit chips in the chip mount area of the flexible lead extending from the main display are positioned in a staggered meshing relation within the opening of the frame. (Kweon Fig. 3)

Kweon differs from the claimed invention by not explicitly reciting the at least one portion of the chip mount area of the flexible lead having a group of electronic circuit chips oppose the at least one portion of the chip mount area free of a group of electronic circuit chips and the at least one portion of the chip mount area of the flexible lead having a group of electronic chips oppose the at least one portion of the chip mount area free of a group of electronic circuit chips.

In an analogous art, document 59-78654 teaches a flexible circuit board where taller and shorter groups of chips are mounted in a staggered relation to each other (Claim 1, Page 3 lines 10-20 and Fig. 3) with at least one portion of the chip mount area of the flexible lead having a group of electronic circuit chips (Fig. 3 [2]) oppose the at least one portion of the chip mount area free of a group of electronic circuit chips (Fig. 3 [To the right of device 2]) and the at least one portion of the chip mount area of the flexible lead having a group of electronic chips oppose the at least one portion of the chip mount area free of a group of electronic circuit chips. (Fig. 3 [First and second upside-down U shape chip mount area empty space across from chip 6]) At the time the invention was made, it would have been obvious to one of ordinary skill in the art to implement the LCD mounting arrangement of Kweon after modifying it to incorporate the flexible chip mounting surface and the staggered chip-mounting pattern of document 59-78654. One of ordinary skill in the art would have been motivated to do this since making portable electronic devices thinner allows them to be more convenient for the consumer to carry.

Further, it is noted that there is a limited amount of space and a finite number of operational parts to be functionally placed within said space of a foldable electronic device and it is well within the scope of one of ordinary skill in the art to find the combination of mounting locations (possibly through trial and error) that allows for the dissipation of heat (LCD driver circuit chips [*i.e.* amplifiers] should not be mounted directly above/below each other because it can stifle heat dissipation) in order to make the device as thin as possible to be aesthetically pleasing and convenient for the user to carry.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MATTHEW SAMS whose telephone number is (571)272-8099. The examiner can normally be reached on M-F 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lester Kincaid can be reached on (571) 272-7922. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

MCS
10/13/2008

/Lester Kincaid/
Supervisory Patent Examiner, Art Unit 2617